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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/596,944	06/29/2006	Robert Lee Maziasz	SC12656TS	2642

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EXAMINER	
SANDOVAL, PATRICK	
ART UNIT	PAPER NUMBER
2825	

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09/30/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/596,944	MAZIASZ ET AL.	
	Examiner	Art Unit	
	PATRICK SANDOVAL	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 September 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *36-45 and 71-79* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *36-45 and 71-79* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This is a response to the papers filed on 9/7/2010.

2. The previous rejections have been withdrawn; however, new grounds of rejection have been cited in this office action in view of further consideration.

3. Claims 36-44 and 71-78 have been amended to address claim objections set forth in the Office Action mailed 7/7/2010. Claim 46 has been cancelled. Claims 36-45 and 71-79 are pending.

Response to Amendment

4. Applicant's arguments with respect to claims 36-45 and 71-79 have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

5. Pursuant to claim 39, insert --portion-- before "of the first logical device" for clarity.

6. Pursuant to claim 77, replace "claim 47" with --claim 36-- for proper claim dependency.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 36-45 and 71-79 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Pursuant to independent claim 36, the limitations "the first portion" (see line 5) and "the third portion (see line 19) lack proper antecedent basis. In line 5, the Examiner suggests replacing "the first portion" with --the portion of the first transistor--. In line 19, the Examiner suggests replacing "the third portion" with --the portion of the second transistor--.

10. Pursuant to claim 41, the limitation "the portion" lacks proper antecedent basis. The Examiner suggests inserting --of the first transistor-- after "the portion".

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. **Claims 36-41, 43-46, 71-75 and 77-79 are rejected** under 35 U.S.C. 103(a) as being unpatentable over Shinomiya et al. (Shinomiya) (US 5,852,562) in view of Maziasz et al. (Maziasz) (US 6,209,123).

13. Shinomiya discloses

14. (Claims 36 and 79) A method comprising:

during compaction of a circuit layout determining at a computer device a first direction associated with the circuit layout (Shinomiya, Fig. 17 # S11, Col. 12, ll. 45-59, based on a determined cell row height);

selecting at the computer device a portion of a first transistor in response to determining the portion of the first transistor extends outward in a first direction from a

first logical device of the circuit layout, the first logical device comprising the first transistor (Shinomiya, Fig. 17 # S12, Fig. 19, Col. 13, ll. 7-37, wherein a big transistor may need to be folded during vertical compaction because of cell row height limitation);

in response to selecting the portion of the first transistor, reshaping at the computer device the first transistor to reduce a size of the first logical device in the first direction (Shinomiya, Fig. 17 # S12, Fig. 19, Col. 13, ll. 7-37, wherein a big transistor is folded during vertical compaction because of cell row height limitation);

reshaping at the computer device a portion of the first logical device in response to reducing the size of the first logical device (Shinomiya, Fig. 17 # S12, Fig. 19, Col. 13, ll. 7-37, Col. 14, ll. 1-9, wherein a big transistor is folded during vertical compaction because of cell row height limitation, resulting in multiple transistor folds or fingers);

15. Shinomiya discloses either vertical or horizontal layout compaction through folding or unfolding of transistors (Shinomiya, Col. 13, ll. 61-67 – Col. 14, ll. 1-9 and 14-19, transistor folding or unfolding to adjust height and width, Col. 15, ll. 11-16, vertical or horizontal layout compaction) but does not explicitly disclose both horizontal and vertical compaction, and thus does not disclose the limitations of:

determining at the computer device a second direction associated with the circuit layout, the second direction different from the first direction;

selecting at the computer device a portion of a second transistor of the circuit layout in response to determining the portion of the second transistor extends outward in the second direction from a second logical device of the circuit layout, the second logical device comprising the second transistor;

in response to selecting the portion of the second transistor, reshaping at the computer device the portion of the second transistor to reduce a size of the second logical device in the second direction;

reshaping at the computer device a portion of the second logical device in response to reducing the size of the second logical device.

16. Maziasz discloses compaction of a design layout to meet height constraints, wherein for example after meeting a desired cell height through compaction in a Y direction, further compaction in an X direction (which is different than the Y direction) is then performed on the circuit layout (Maziasz, Col. 14, ll. 24-67 – Col. 15, ll. 1-2).

17. It would have been obvious to one of ordinary skill in the art to compact a layout design in both Y and X directions in order to provide for the most efficient area utilization possible (Maziasz, Col. 14, ll. 24-35).

18. The combination of Shinomiya in view of Maziasz further discloses:

19. (Claim 37) Wherein the portion of the first transistor comprises a first transistor finger (Shinomiya, Figs. 20-21 and applicable text, wherein transistor folding adds fingers while unfolding removes fingers).

20. (Claim 38) Wherein the portion of the first logical device comprises a second transistor finger of the first transistor (Shinomiya, Figs. 20-21 and applicable text, wherein transistor folding adds fingers while unfolding removes fingers).

21. (Claim 39) Wherein the portion of the first logical device comprises a transistor finger of a second transistor (Shinomiya, Figs. 20-21 and applicable text, wherein transistor folding adds fingers while unfolding removes fingers).

22. (Claims 40) Wherein reshaping the portion of the first transistor comprises reducing a size of the first transistor finger (Shinomiya, Figs. 20-21 and applicable text, wherein transistor folding adds fingers while unfolding removes fingers).

23. (Claims 41) Wherein reshaping the portion of the first transistor comprises removing the first transistor finger (Shinomiya, Figs. 20-21 and applicable text, wherein transistor folding adds fingers while unfolding removes fingers).

24. (Claim 43) Reshaping the portion of the first logical device in response to reducing the size of the portion of first transistor (Shinomiya, Figs. 20-21 and applicable text, wherein transistor folding adds fingers while unfolding removes fingers).

25. (Claims 44 and 45) Storing a first state associated with the circuit layout at the computer device in response to selecting the portion of the first transistor;

in response to reshaping the portion of the first transistor, determining if a size of the circuit layout has been reduced in the first direction (Maziasz, Fig. 9 and applicable text) (Shinomiya, Figs. 17 and 19 and applicable text); and

in response to determining the size of the circuit layout has not been reduced, restoring the circuit layout to the first state (Maziasz, Fig. 9 and applicable text, wherein compaction in a Y direction is first as there would be no reason to compact in the X direction following if the Y direction constraints are not yet met) (Shinomiya, Figs. 17 and 19 and applicable text) (wherein it is implicit in layout optimization that if a proposed solution does not meet cell height constraints it would not be a valid solution).

26. (Claim 71) Wherein the portion of the second transistor comprises a first transistor finger (Shinomiya, Figs. 20-21 and applicable text, wherein transistor folding adds fingers while unfolding removes fingers).

27. (Claim 72) Wherein the portion of the second logical device comprises a second transistor finger of the first transistor (Shinomiya, Figs. 20-21 and applicable text, wherein transistor folding adds fingers while unfolding removes fingers).

28. (Claim 73) Wherein the portion of the seconds logical device comprises a second transistor finger of the second transistor (Shinomiya, Figs. 20-21 and applicable text, wherein transistor folding adds fingers while unfolding removes fingers).

29. (Claim 74) Wherein reshaping the portion of the second transistor comprises reducing a size of the second transistor finger (Shinomiya, Figs. 20-21 and applicable text, wherein transistor folding adds fingers while unfolding removes fingers).

30. (Claim 75) Wherein reshaping the portion of the second transistor comprises removing the first transistor finger (Shinomiya, Figs. 20-21 and applicable text, wherein transistor folding adds fingers while unfolding removes fingers).

31. (Claim 77) Wherein the portion of the second transistor comprises a first transistor finger (Shinomiya, Figs. 20-21 and applicable text, wherein transistor folding adds fingers while unfolding removes fingers).

32. (Claim 78) Wherein reshaping the portion of the second transistor comprises reducing a size of the second transistor finger (Shinomiya, Figs. 20-21 and applicable text, wherein transistor folding adds fingers while unfolding removes fingers)s.

33. **Claims 42 and 76 are rejected** under 35 U.S.C. 103(a) as being unpatentable over Shinomiya et al. (Shinomiya) (US 5,852,562) in view of Maziasz et al. (Maziasz) (US 6,209,123), further in view of Wang, L. Y. et al. (Wang), "Topological cell compaction via transistor rotation", 1991, Circuits and Systems, Vol. 2, Pages 909-912.909-912.

34. Shinomiya in view of Maziasz discloses all of the elements of claim 36 from which claims 42 and 76 depend.

35. Shinomiya in view of Maziasz does not disclose:

a. (Claim 42) Wherein reshaping the portion of the first transistor comprises rotating the first transistor; and

b. (Claim 76) Wherein reshaping the portion of the second transistor comprises rotating the second transistor.

36. Wang discloses topological layout compaction inclusive of transistor rotation to change the layout topology (Wang, Page 910, Section 3).

37. It would have been obvious to one of ordinary skill in the art the addition of transistor rotation would provide for increased compaction options and flexibility for layout optimization.

Remarks

38. The objections to claims 36 and 46 and the rejection of claims 36-46 and 71-79 under 35 USC 112 have been removed in light of Applicant's claim amendments filed 9/7/2010. However, new claim objections and new claim rejections under 35 USC 112

have also been made in response to Applicant's claim amendments (see claim objections and rejections above).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PATRICK SANDOVAL whose telephone number is (571)272-7973. The examiner can normally be reached on 8:00 am to 5:30 pm Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Paul Dinh/
Primary Examiner, Art Unit 2825

/Patrick Sandoval/
Examiner, Art Unit 2825